Daniel Andrasz

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EDUCATION

University of Illinois at Urbana-Champaign Expected May 2027
Bachelor of Science in Materials Science & Engineering 3.57 GPA
Minors in Semiconductor Engineering & Electrical and Computer Engineering (ECE)

- **Relevant Coursework:** Compound Semiconductors and Devices, IC Device Theory & Fabrication, Electronic Properties of Materials, Digital Systems Laboratory, Computer Organization and Design, Quantum Systems I

WORK EXPERIENCE

University of Illinois Urbana-Champaign Champaign, Illinois
Teaching Assistant, Digital Systems Laboratory (ECE 385) January 2026 – Present

- Guided 200+ students on FPGA-based digital system design, SystemVerilog RTL implementation, and Vivado synthesis workflows

University of Illinois Urbana-Champaign Champaign, Illinois
Research Assistant, Photonic Systems Laboratory August 2025 - Present

- Conducted exploratory research on p++/intrinsic silicon bonding and interface characterization using I-V/C-V measurements to identify interface defects
- Assisted with semiconductor fabrication techniques such as photolithography, wet and dry etching, and thin-film deposition using a mask aligner and plasma etcher
- Analyzed device performance using I-V/C-V electrical characterization and material analysis, processing data with Python scripts, and guided design refinements

Texas A&M University College Station, Texas
Research Assistant, Thermal Engineering Group May 2025 – August 2025

- Fabricated microscale thermal devices in Class 100 cleanroom using 4-step microfabrication process, achieving 5 µm resolution and 90% yield
- Validated the thermal test vehicle across a 300K - 400K temperature range, confirming operation within 5% of design specifications using 4-point probe measurements

University of Illinois Urbana-Champaign Champaign, Illinois
Teaching Assistant, Computer Systems & Programming (ECE 220) August 2024 – Present

- Mentored 300+ students in C, C++, and Assembly each semester, managing 5+ lab sections and reducing average debugging time per student through targeted logic analysis

PROJECTS

NES Hardware Emulator on FPGA
C++, SystemVerilog, Microarchitecture, Graphics Pipeline, Static Timing Analysis

- Architected a cycle-accurate NES emulator in SystemVerilog running at 21.47 MHz, supporting commercial ROMs at 60 FPS with zero frame drops
- Implemented a PPU graphics pipeline handling 64 sprites per scanline and full palette management while meeting 10ns static timing constraints
- Integrated a USB HID host interface to poll gamepads at 1 kHz, translating button states into low-latency NES joypad input signals

CMOS Integrated Circuit Wafer
Cleanroom, Photolithography, Diffusion, Metrology

- Fabricated NMOS/PMOS devices using a 5-mask process (oxidation, lithography, diffusion, metallization) with variable channel lengths
- Conducted wafer-level probing on 50+ devices achieving 75% yield; correlated failures to diffusion anomalies via I-V analysis

Semiconductor Compact Model Extraction Framework
Python, PyTorch, Streamlit, SciPy, Semiconductor Physics

- Architected a hybrid physics-ML extraction framework (1,500+ lines of Python) for diode and MOSFET devices, leveraging PyTorch neural networks to predict initial conditions and accelerate non-linear least squares optimization
- Engineered a robust global optimization engine to extract unified physical parameters simultaneously across complex datasets, including multi-temperature I-V, C-V, and MOSFET output/transfer characteristic families

SKILLS

- **Semiconductor Fabrication:** Photolithography (Mask/Maskless), E-beam Evaporator, Wet/Dry Etching (HF/BOE/RIE), Thermal Oxidation, Spin Coating, Lift-off, Diffusion, Contact Annealing
- **Characterization & Metrology:** I-V/C-V Profiling, Parameter Extraction, 4-Point Probe, Probe Station Operation
- **Programming & Tools:** Python (NumPy, SciPy, Pandas, Matplotlib, Streamlit), C, C++, SystemVerilog, Assembly, Java, Bash, LaTeX, Xilinx Vivado, Intel Quartus, ModelSim/Questa, GitHub, Linux (WSL/Ubuntu), SolidWorks, GDB